Atari TT030 VME Expansion

The VME expansion slot in the TT030 supports a single height VME card (3U Eurocard format) which is A24/D16 or A16/D16 compatible. The slot supports slave cards only. The connector and board mechanical dimensions comply with the VITA C.1 VME bus specification.

The slot is electrically compatible with the VME specification, but please note the following points:

No bus arbitration is supported. BR0*, BR1*, BR2*, and BR4* are connected together and pulled up by a 1K resistor to VCC. BG0IN*, BGG1IN*, BG2IN*, and BG3IN* are connected together and pulled up by a 1K resistor to VCC. BBSY* and BCLR* are each pulled up by a 1K resistor to VCC but are not otherwise driven. BG0OUT, BG1OUT, BG2OUT, and BG3OUT are not connected.

The interrupt lines IRQ1* thru IRQ7* can each be used and are pulled up by a 1K resistor to VCC. IRQ3*, IRQ5*, and IRQ6* can also be driven low by the system. The SYSFAIL* signal is also pulled up by a 1K resistor and can generate a level 7 system interrupt when asserted by a card. IACK* and IACKIN* are driven by the system. A card should not drive these signals. IACKOUT* is not connected. The status word supplied by the card during the interrupt acknowledge cycle is used as the 68030 interrupt vector. For compatibility with Atari products, the vector supplied must not be OxFF. All VME bus and system interrupts are independently maskable in the SCU.

SYSCLK is driven with a 16.107953 MHz clock in the TT030. SERCLK and SERDAT* are not connected. The ACFAIL* signal is driven low by the system when the power supply is not stable. ACFAIL* will be asserted 1 MS before the supply leaves the regulated range. It is pulled up by a 1K resistor.

AM0, AM1, AM2, and AM4 are driven by the system. AM3 and AM5 are connected together and pulled up by a 1K resistor to VCC. This implementation allows Standard Supervisory and Non-Priviliged Program and Data accesses and Short Supervisory and Non-Priviliged Accesses. Block Transfers are not supported. LWORD* is pulled up by a 1K resistor but not otherwise driven.

The BERR* and SYSRES* signals are connected directly to the system bus error and reset signals. The bus error timer implemented on the system board will time out and generate a bus error if the card does not assert DTACK* within 255 cycles of 16MHz after the VME AS* falls. The SYSRES* generated when the 68030 executes a Reset instruction may be as short as 16uS long. They are pulled up by 1.2K resistors and can be driven low by the system as well as by the card. The +5VSTDBY signal is connected to +5V. DTACK* is pulled up by a 1K resistor.

DMA/BUS MASTERSHIP PRIORITIES

DMA PRIORITIES

priority	function
highest	
	ACSI/Floppy Controller
	SCC DMA Controller
	SCSI DMA Controller
lowest	

All other signals on the connectors comply with VME functionality, but with electrical limitations on current drive and termination. There is no termination in the system other than the pullups mentioned above. All outputs have at least 1 LS TTL drive capability and no input presents more than 2 LS TTL loads.

On the TT030, just under the entire 16Mb A24 space is available:

FEOO OOOO	- FEFF FFFF	A24:D16, VME card sees least significant 24 bits of address
FEFF OOOO	- FEFF FFFF	A16:D16

Third parties should design their cards to have strappable or programmable addresses, interrupt priorities, and interrupt vectors. It is good design practice to decode the address space as completely as possible. The A16 space is particularly sensitive.

Third parties should provide interrupt status bytes in the range 0x80-0xBF (i.e. vectors between 0x200 and 0x2FF).

Power available for the VME card:

Voltage	Max Current	Regulation	Ripple/Noise (pk-to-pk)
+5V	2.0A	+5%/-4%	60 mV
+12V	50MA	+/-5%	120 mV
-12V	50MA	+/-10%	120 mV